CLAIMS

1. An operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising:

a register array having plural registers each for holding an arbitrary value based on a write address and a write control signal and outputting this value based on a read address;

an operation portion for performing operation on a value read from said register array;

an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion; and

an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion,

wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction; and

wherein based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another register.

2. The operation-processing device according to claim 1, comprising a read only memory cell in which said operation program is stored.

3. The operation-processing device according to claim 1, wherein said operation program includes operation instruction to perform the register-to-register addressing processing.

4. The operation-processing device according to claim 1,

wherein said register array and the read only memory are comprised of plural memory cells;

wherein said operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of plural arithmetic/logic operation elements; and

wherein said memory cells and the arithmetic/logic operation elements are constituted of a programmable logic devices formed on the identical semiconductor chip.

5. The operation-processing device according to claim 1, wherein said instruction execution-controlling portion has:

a first selector for selecting any one of a read execution address to select said one register and a read address to select this register again; and

a second selector for selecting any one of a write execution address to select said one register and a write address to select this register again.

6. A constructing method for constructing a device for performing operation processing based on an arbitrary operation program, said method comprising the steps of:

forming plural memory cells and arithmetic/logic operation elements on the same semiconductor chip beforehand;

combining said memory cells to define a register array and a read only memory and combining said arithmetic/logic operation elements to

define an operation portion, an instruction-decoding portion, and an instruction-execution-controlling portion; and

connecting said register array, the read only memory, the operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion to each other based on preset wiring information and writing an arbitrary operation program to said read only memory.

7. The constructing method for constructing an operation-processing device according to claim 6, wherein said operation program includes operation instruction to perform the register-to-register addressing processing.

8. The constructing method for constructing an operation-processing device according to claim 6, comprising the steps of:

providing a rewritable nonvolatile storage device for storing said wiring information;

upon power application, reading the wiring information from said storage device; and

based on said set wiring information, interconnecting the register array, the read only memory, the operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion.

9. The constructing method for constructing an operation-processing device according to claim 6, wherein the wiring information stored in said storage device is rewritten on demand in accordance with functions of the operation-processing device.

10. The constructing method for constructing an operation-processing device according to claim 6, wherein said register array has plural registers each for holding an arbitrary value based on a write address and a write control signal and outputting this value based on a read address.

11. The constructing method for constructing an operation-processing device according to claim 6, wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction; and

wherein based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another register.

12. The constructing method for constructing an operation-processing device according to claim 6, wherein said instruction-execution-controlling portion comprises:

a first selector for selecting any one of a read execution address to select said one register and a read address to select this register again; and

a second selector for selecting any one of a write execution address to select said one register and a write address to select this register again.

13. The constructing method for constructing an operation-processing device according to claim 6, wherein said operation portion performs operation on a value read from said register array;

wherein said instruction-decoding portion decodes an operation instruction from on an operation program for operating said operation portion; and

wherein said instruction-execution-controlling portion controls said register array and the operation portion in order to execute the operation instruction decoded by said instruction-decoding portion.

14. An operation-processing method for performing operation processing based on an arbitrary operation program, said method comprising the steps of:

beforehand preparing plural registers each for holding an arbitrary value based on a write address and a write control signal and outputting this value based on a read address;

thereafter decoding an operation instruction from said operation program;

selecting one of said registers based on said operation instruction;

performing register-to-register addressing processing for selecting, based on a value held by said selected register, another register and selecting said another register based on said operation instruction; and

performing operation on a value held by said selected another register and a value of the register selected by said register-to-register addressing processing.

15. The operation-processing method according to claim 14, wherein a result of said operation is stored in the register selected on the basis of the value held by said register.

16. The operation-processing method according to claim 14, wherein said operation program includes operation instruction to perform said register-to-register addressing processing.

17. An operation-processing device for performing operation processing based on an operation program for performing register-to-register addressing processing, comprising:

plural registers;

a storage portion for storing a compressed program having a different instruction length in which the number of bits of a instruction for specifying the register is reduced beforehand based on a frequency at which said registers are used and a type of each of the registers is written in an instruction structure of said program;

an instruction-decoding portion for reading the compressed program from said storage portion to decode the type of each of the registers and, based on this type of the registers, restore the number of bits of the instruction for specifying said register; and

an instruction execution/operation portion for performing an arbitrary operation by specifying said register based on the instruction having a predetermined length restored by said instruction-decoding portion.

18. The operation-processing device according to claim 17, wherein in a case where N number of registers are used, when said N number of registers are assigned serial numbers of 1 through N, the types of the registers are classified into a group having a higher use frequency of

said first through K'th registers and a group having a lower use frequency of said (K+1)'th through N'th registers.

19. An operation-processing method for performing operation processing based on an operation program for performing register-to-register addressing processing, said method comprising the steps of:

storing a compressed program having a different instruction length in which the number of bits of an instruction for specifying the register is reduced beforehand based on a frequency at which said register is used and a type of said registers are written in an instruction structure of said program;

reading the compressed program to decode the register type;

based on this register type, restoring the number of bits of the instruction for specifying said register; and

performing an arbitrary operation by specifying the register based on the restored instruction having a predetermined length.

20. The operation-processing method according to claim 19, wherein in a case where N number of registers are used, when said N number of registers are assigned serial numbers of 1 through N, the types of the registers are classified into a group having a higher use frequency of said first through K'th registers and a group having a lower use frequency of said (K+1)'th through N'th registers.

21. An operation-processing system comprising:

a program creation device for creating a program by editing an instruction for performing register-to-register addressing operation, based on a predetermined programming language on one hand; and

an operation-processing device for performing the register-to-register addressing operation by using said program and plural registers on the other hand,

wherein said program creation device reduces the number of bits of an instruction for specifying the register based on a frequency at which said registers are used and writes a type of each of the registers in an instruction structure of the program, thereby creating a compressed program having a different instruction length; and

wherein said operation-processing device obtains the compressed program created by said program creation device to decode the type of each of the registers and, based on said register type, restores the number of bits of the instruction for specifying the register, to specify the plural registers based on the instruction having a predetermined length, thereby performing arbitrary operation.

22. The operation-processing system according to claim 21, wherein said operation-processing comprises:

plural registers;

a storage portion for storing a compressed program for specifying said register;

an instruction-decoding portion for reading the compressed program from said storage portion to decode the type of each of the registers and, based on this type of each of the registers, restoring the number of bits of the instruction for specifying said register; and

an instruction execution/operation portion for performing an arbitrary operation by specifying said register based on the instruction having a predetermined length restored by said instruction-decoding portion.

23. The operation-processing system according to claim 21, wherein in a case where N number of registers are used, when said N number of registers are assigned serial numbers of 1 through N, the types of the registers are classified into a group having a higher use frequency of said first through K'th registers and a group having a lower use frequency of said (K+1)'th through N'th registers

24. An operation-processing method comprising the steps of:

creating, at a program creation system, a program by editing an instruction for performing register-to-register addressing operation based on a predetermined programming language; and

performing, at a program execution system, said register-to-register addressing operation by using this program and plural registers,

wherein said program creation system reduces the number of bits of an instruction for specifying the register based on a frequency at which said registers are used and writes a type of each of the registers in an instruction structure of this program, thereby creating a compressed program having a different instruction length; and

wherein said program execution system obtains the compressed program created by said program creation system to decode the type of each of the registers, based on said decoded register type, restores the number of bits of the instruction for specifying the register, and specifies the plural registers based on said instruction having a restored predetermined length, thereby performing arbitrary operation.

25. The operation-processing method according to claim 24, wherein in a case where N number of registers are used, when said N number

of registers are assigned serial numbers of 1 through N, the types of the registers are classified into a group having a higher use frequency of said first through K'th registers and a group having a lower use frequency of said (K+1)'th through N'th registers.